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TITLE: LINER MASK FOR SEMICONDUCTOR APPLICATIONS

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LINER MASK FOR SEMICONDUCTOR APPLICATIONS

BACKGROUND OF THE INVENTION

1. Technical Field

[0001] The present invention generally relates to semiconductor applications. In particular, the present invention relates to methods, processes, systems for producing a liner mask on a semiconductor structure and corresponding applications.

2. Related Art

[0002] Although applicable in principle to any integrated circuit, the present invention and the problem area on which it is based are explained with regard to integrated memory circuits in silicon technology.

[0003] In a prior art patent application DE 102 55 845.0, the production of a liner mask in a trench by means of an implantation of boron ions in definite regions in an amorphous silicon liner and following selective wet etching in NH_4OH is disclosed.

[0004] For the known method, the fact that the selectivity between an amorphous non-implanted silicon and the amorphous implanted silicon having only a factor 8-10 has been found to be a disadvantage. This leads to increasing aspect ratios and decreasing liner layers dispersion phenomena appearing at the

implantation cause an implantation of unwished regions and thereby a mask erosion on this unwished regions at the following etching.

[0005] In particular, the sequential execution of several implantation steps, for example with the same inclination opposite the vertical axis and different rotations angles around the vertical axis, the dispersion probability is increased and thereby the above-mentioned problems are increased.

[0006] Accordingly, there is a need for a method for producing a liner mask on a semiconductor structure that is less vulnerable to above-mentioned dispersion problems.

BRIEF SUMMARY

[0007] The above problems have been solved with the present invention. By way of introduction only, an object of the present invention is to specify a method for producing a liner mask on a semiconductor structure that is less vulnerable to above-mentioned dispersion problems.

[0008] According to the invention, this object may be achieved by a method for producing a liner mask on a semiconductor structure including providing an amorphous liner layer on a top side of the semiconductor structure in a deposition process at a first temperature; annealing the amorphous liner layer at a second temperature, which is higher than the first temperature; performing an implantation of extrinsic ions in a subregion of the at least semi-crystalline liner layer for decreasing the etching rate of the subregion in the predetermined

etchant and creating a etch selectivity between the subregion complementary subregion and the subregion in the predetermined etchant; and selectively removing of the to the subregion complementary subregion opposite to the subregion in a etching step in the predetermined etchant for completing the liner mask

[0009] An object of the present invention may be achieved by means of an application of a use of a liner mask for a trench capacitor with an isolation collar in a substrate that is single-sided electrically connected with the substrate by means of a buried contact, in particular for a semiconductor memory cell with a planar selection transistor provided in the substrate and connected over the buried contact, whereas the liner mask is produced for defining a single-sided contact region and an other-sided isolation region of the buried contact in a trench for the trench capacitor.

[0010] An advantage of the method and its application according to the invention is an increase in the selectivity for producing a liner mask to be many times higher than the prior art.

[0011] The present invention may include an annealing step for increasing the crystallization degree of the liner layer before an implantation step. Due to increase in selectivity, removing the non-implanted liner region by means of the etching step that follows the implantation step becomes easier. Thus, the dispersion phenomena do not have such a high impact, and the mask erosion may be prevented.

[0012] In accordance with an embodiment, the liner layer consists of silicon, whereas the extrinsic ions are boric ions or boron ions.

[0013] In accordance with an embodiment, the semiconductor structure comprises a trench, whereas the implantation is made in such a manner that the complementary subregion lies in the trench.

[0014] In accordance with an embodiment, the first temperature is between approximately 400°C and 600°C, and the second temperature lies between approximately 700°C and 1100°C.

[0015] In accordance with an embodiment, a further liner layer is provided on the top side of the semiconductor structure underneath a liner layer, whereas on the further liner layer the etching step for the selective removal of the complementary subregion stops.

[0016] The foregoing discussion of the summary is provided only by way of introduction. Other systems, methods, processes, apparatuses, features and advantages of the invention will be, or will become, apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods, features and advantages be included within this description, be within the scope of the invention, and may be realized and obtained by means of the instrumentalities and combinations particularly pointed out in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The invention can be better understood with reference to the following drawings and description. The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention. Moreover, in the figures, like referenced numerals designate corresponding parts throughout the different views.

[0018] Figs. 1A and 1B show schematic views of method steps for producing a liner mask on a semiconductor structure as an embodiment according to the present invention;

[0019] Figs. 2A-2G show schematic views of method steps for producing a liner mask on a semiconductor structure as a second embodiment according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0020] Exemplary embodiments of the invention are illustrated in the drawings and explained in more detail in the description below.

[0021] Fig. 1A and 1B are schematic views of successive method steps of a method for producing a liner mask on a semiconductor structure as a first embodiment according to the invention.

[0022] In Fig. 1A, reference symbol 5 designates a trench provided in the silicon semiconductor substrate 1. On the top side OS of the semiconductor substrate 1, a silicon nitride liner layer 50 and an underneath lying silicon liner

layer 55 of amorphous undoped silicon are provided, (e.g. with a CVD-step at 500°C.)

[0023] Then, in a separate fast annealing step, the silicon liner 55 may be tempered at 900°C for 30 seconds in N_2 to increase its crystallization degree and thereby its etching rate in NH_4OH.

[0024] Afterwards, with reference to Fig. 1B, it follows an inclined implantation I1 with a predetermined angle opposite of the vertical axis, (e.g. 30°), whereas BF_2 is implanted at an energy 10 keV with a dose of $3x10^{14}$ cm^{-2} in the subregion 55a of the silicon liner 55 and the region 55b remains shadowed against the implantation. Thus, the etching characteristics of the boron-contaminated region 55a of the silicon liner 55 changes, which is utilized according to Fig. 1B, with selectively removing of the region 55b by means of an adequate wet etching step in NH_4OH for uncovering the underneath lying silicon nitride liner layer 50 on which the wet etching step in NH_4OH stops.

[0025] The selectivity between the (partially) crystalline implanted silicon layer region 55a and the (partially) crystalline non-implanted silicon liner region 55b at the wet etching step amounts to 63,4 at the mentioned example.

[0026] Thus, a liner mask is produced from the liner 55, by means of which further selective etching steps in the underneath lying semiconductor structure can be done.

[0027] Figures 2A-2G are schematic views of successive method steps of a method for producing a liner mask on a semiconductor structure as a second embodiment according to the invention.

[0028] In Figure 2A, reference symbol 5 designates a trench provided in the silicon semiconductor substrate 1. On the top side OS of the semiconductor substrate 1, a hardmask is provided consisting of a pad oxide layer 2 and a pad nitride layer 3. In the lower and middle region of the trench 5, a dielectric 30 is provided which isolates an electrically conductive filling 20 opposite to the surrounding semiconductor substrate 1.

[0029] In the upper and middle region of trench 5, a revolving isolation collar 10 is provided that is exactly deepened in the trench 5 like the conductive filling 20. For example, a material for the isolation collar 10 is silicon oxide, and a material for the electrically conductive filling 20 is polysilicon. But, of course, other materials may be used.

[0030] In addition, a conductive filling 40 embedded under the top side OS and consisting of epi-polysilicon is provided. Thus, the conductive filling 40 describes a circumferentially connected buried contact that has to be partially removed for forming an isolation region IS later. As to realize the single-sided connection of the region 40 to the semiconductor substrate 1, the below-mentioned "subtractive" method steps are performed.

[0031] In accordance with Fig. 2B, on the top side OS' of the semiconductor structure, a silicon nitride liner layer 50 and a above-lying silicon liner layer 55 of amorphous undoped silicon are provided, (e.g., in a CVD step at 500°C).

[0032] Then, in a separate fast annealing step, the silicon liner 55 is tempered at 900°C for 30 s in N_2 for increasing the crystallization degree and thereby the etching rate in NH_4OH.

[0033] In accordance with Fig. 2C, it follows in the following an inclined implantation I1 with a predetermined angle opposite to the vertical axis, (e.g. 30°), whereas BF_2 at an energy 5 keV with a dose of $3x10^{14}$ cm^{-2} is implanted in the region 55a of the silicon liner 55, and a region 55b remains shadowed against the implantation. Thus, the etching characteristics of the boron-contaminated region 55a of the silicon liner 55 changes which is utilized, in accordance with Fig. 2D, for selectively removing the region 55b by means of an adequate wet etching step in NH_4OH in order to uncover the silicon nitride liner layer 50 lying underneath on which the wet etching step in NH_4OH stops.

[0034] The selectivity between the (partially) crystalline implanted silicon liner region 55a and the (partially) crystalline non-implanted silicon liner region 55b at the wet etching step amounts to 63,4 at the example mentioned above.

[0035] Thus, a liner mask is produced from the liner 55, by means of which further selective etching steps in the underneath-lying semiconductor substrate in accordance with Figures 2E-2G can be performed.

[0036] In accordance with Fig. 2E, it follows a wet oxidation of the remaining implanted region 55a of the liner 55 getting a adequate oxidized liner region 55". In the following process step, a part of the silicon nitride liner 50 is removed from the surface of the conductive region 40 and from the side wall of the trench 5 or of the hardmask 2, 3 by use of the oxidized implanted region 55" of the liner 55.

[0037] In accordance with Fig. 2F, it follows in the following an etching of the conductive filling 40 and of a part of the conductive filling 20 by use of the region 55" as a mask.

[0038] Thus, in the process state as shown in Fig. 2F, a part of the region 40 being used as a buried contact is removed, and then, at the adequate place, an adequate to the top and to the side isolating oxide filling 45 can be provided by means of depositing and back-etching in the further proceeding of the method, after the liners 50, 55 (55") have been removed from the surface, as is shown in Fig. 2G. This forms a buried contact with the connection region KS and the isolation region IS.

[0039] Although the present invention has been described above on the basis of a preferred exemplary embodiment, it is not restricted thereto, but rather can be modified in diverse ways.

[0040] In particular, the selection of the layer materials is only by way of example and can be varied in many different ways.

[0041] Although the annealing step in the above-mentioned example was conducted at approximately 900°C, one or more temperatures are possible in the range of 700°C -1100°C. Also, the deposition temperature of the liner layers can lie in the range of approximately 400°C -600°C, although it amounts to 500°C in the above-mentioned example.

[0042] While the above embodiments have been described, those skilled in the art will recognize that the advantages may be extended to various semiconductors and various processes. Accordingly, the invention is not to be restricted except in light as necessitated by the accompanying claims and their equivalents.

LIST OF REFERENCE SYMBOLS

[0043]	1	Si-semiconductor substrate
[0044]	OS, OS'	top side
[0045]	2	pad oxide
[0046]	3	pad nitride
[0047]	5	trench
[0048]	40	conductive epitaxial region
[0049]	10	isolation collar
[0050]	20	conductive filling (e.g. polysilicon)
[0051]	30	capacitor dielectric
[0052]	KS	contact region
[0053]	IS	isolation region
[0054]	50	silicon nitride liner
[0055]	55	liner of amorphous undoped silicon
[0056]	55a	implanted region of 55
[0057]	55b	shadowed region of 55
[0058]	55''	oxidized implanted region of 55b
[0059]	I1	implantation